Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-27 (Canceled)

28. (Previously Presented) A non-volatile semiconductor memory device comprising:

a memory cell array including a plurality of memory cells arranged in a matrix;

a word line connected to two or more of the memory cells arranged in a row direction;

a source line connected to two or more of the memory cells;

a row decoder circuit configured to supply a write verify voltage to the word line;

a plurality of bit lines each connected to two or more of the memory cells arranged in a column direction; and

a plurality of bit line control circuits each being provided for at least one of the bit lines, and each storing data of a first logic level or a second logic level,

wherein the bit line control circuit storing data of the first logic level performs a detection operation for detecting a written state of a first memory cell corresponding to the bit line control circuit storing data of the first logic level after a predetermined period from completion of a charging operation for charging a first bit line corresponding to the bit line control circuit storing data of the first logic level, and

during the predetermined period, a first voltage is supplied to a second bit line corresponding to the bit line control circuit storing data of the second logic level.

29. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein a voltage level of the source line is different from the first voltage.

30. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein a voltage level of the source line is higher than the first voltage.

31. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein the first voltage is a voltage which is substantially same voltage level of the first bit line just after completion of the charging of the first bit line.

32. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein the first voltage is not higher than a voltage level of the first bit line just after completion of the charging of the first bit line.

33. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein the detection operation is performed in order to judge whether writing of data is completed in a previous write operation in the first memory cell.

34. (Currently Amended) The non-volatile semiconductor memory device according to claim 28, wherein the first voltage is not supplied to the first bit line ~~is not set to the first voltage~~ during the predetermined period.

35. (Currently Amended) The non-volatile semiconductor memory device according to claim 28, wherein the first voltage is not supplied to the first bit line ~~is not set to the first voltage~~ in at least a part of the predetermined period.

36. (Currently Amended) The non-volatile semiconductor memory device according to claim 28, wherein a current path for charging a bit line in the charging operation is different from a current path for ~~setting~~ supplying the first voltage to a bit line ~~to the first voltage~~ in the predetermined period.

37. (Currently Amended) The non-volatile semiconductor memory device according to claim 28, wherein a current path for charging a bit line in the charging operation includes at least one transistor which is not included in a current path for ~~setting~~ supplying the first voltage to a bit line ~~to the first voltage~~ in the predetermined period.

38. (Currently Amended) The non-volatile semiconductor memory device according to claim 28, further comprising:

a first charging circuit performing an operation for charging a bit line in the charging operation; and

a first voltage ~~setting~~ supplying circuit performing an operation for ~~setting~~ supplying the first voltage to the second bit line ~~to the first voltage~~ in the predetermined period,

wherein at least one transistor in the first voltage ~~setting~~ supplying circuit is not included in the first charging circuit.

39. (Currently Amended) The non-volatile semiconductor memory device according to claim 28,

wherein an operation of ~~setting~~ supplying the first voltage to the second bit line ~~to the first voltage~~ is controlled by both a control signal and data stored in the bit line control circuit corresponding to the second bit line.

40. (Currently Amended) The non-volatile semiconductor memory device according to claim 28, further comprising a first voltage ~~setting~~ supplying circuit including a first transistor and a second transistor,

wherein a voltage ~~setting~~ supplying operation for ~~setting~~ supplying the first voltage to the second bit line ~~to the first voltage~~ in the predetermined period is controlled by both a control signal and data stored in the bit line control circuit storing data of the second logic level, the first transistor has an input for the control signal, the second transistor has an input for a first signal reflecting the data stored in the bit line control circuit in the voltage ~~setting~~ supplying operation, and the first and the second transistors are connected to each other.

41. (Currently Amended) The non-volatile semiconductor memory device according to claim 40, wherein the bit line control circuit includes a data latch circuit, the data latch circuit stores data of the first logic level or the second logic level, a voltage level of a first node in the data latch circuit depends on the data stored in the bit line control circuit, and a voltage level of a gate of the second transistor reflects the voltage level of the first node in the voltage ~~setting~~ supplying operation.

42. (Currently Amended) The non-volatile semiconductor memory device according to claim 41, wherein a voltage of the first node is transferred to the gate of the second transistor before or during the voltage ~~setting~~ supplying operation.

43. (Previously Presented) The non-volatile semiconductor memory device according to claim 41, wherein the first node and the gate of the second transistor are connected directly.

44. (Previously Presented) The non-volatile semiconductor memory device according to claim 40, wherein the first and the second transistors are connected in series.

45. (Previously Presented) The non-volatile semiconductor memory device according to claim 44, wherein one end of the first and the second transistors is connected to power supply voltage.

46. (Previously Presented) The non-volatile semiconductor memory device according to claim 44, wherein one end of the first and the second transistors is connected to 0V.

47. (Currently Amended) The non-volatile semiconductor memory device according to claim 40, wherein the second transistor corresponding to the bit line control circuit storing data of the first logic level does not transfer the first voltage in the voltage ~~setting~~ supplying operation, and the second transistor corresponding to the bit line control circuit storing data of the second logic level transfers the first voltage in the voltage ~~setting~~ supplying operation.

48. (Currently Amended) The non-volatile semiconductor memory device according to claim 28, wherein a voltage ~~setting~~ supplying operation for ~~setting~~ supplying the first voltage to the second bit line ~~to the first voltage~~ starts in beginning of the predetermined period.

49. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein the data of the first logic level is "0", and the data of the second logic level is "1".

50. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein a voltage level of the source line is substantially equal to a voltage level of the first voltage in the predetermined period.

51. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein each of the plurality of bit line control circuits includes or is connected to a sense node, a detection result for each of the sense node set to the first voltage is different from a detection result for each of the sense node set to a voltage which is substantially equal to the voltage of the source line set in the predetermined period.

52. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein both the first bit line and the second bit line are charged before the predetermined period.

53. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein the bit line control circuit storing data of the second logic level before the detection operation stores data of the second logic level after the detection operation.

54. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein the bit line control circuit storing data of the first logic level before the detection operation stores data of the first logic level after the detection operation when writing of data into the first memory cell was not completed in a previous write operation.

55. (Previously Presented) The non-volatile semiconductor memory device according to claim 54, wherein the bit line control circuit storing data of the first logic level before the detection operation stores data of the second logic level after the detection operation when the writing of data into the first memory cell was completed in the previous write operation.

56. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein one bit line control circuit is connected to at least two bit lines each of which is connected to the bit line control circuit through at least one transistor, and one of the at least two bit lines is the first bit line which is selected in an operation of charging the bit line and in the detection operation.

57. (Currently Amended) The non-volatile semiconductor memory device according to claim 28,

wherein: each of the plurality of bit line control circuits includes or is connected to a sense node; each of the plurality of bit line control circuits includes a data latch circuit;

~~wherein~~ each voltage level of the sense node is sensed by the corresponding bit line control circuit to determine a detection result in a detection operation, and each of the data latch circuit stores data of the first logic level or the second logic level.

58. (Previously Presented) The non-volatile semiconductor memory device according to claim 57, wherein a voltage level of a first node in each of the data latch circuits depends on data stored in the corresponding bit line control circuit, the sense node is connected to the bit line through at least one transistor, and the sense node is connected to the first node through at least one transistor.

59. (Previously Presented) The non-volatile semiconductor memory device according to claim 57, wherein a voltage level of a first node in each of the data latch circuits depends on the data stored in the corresponding bit line control circuit, the sense node is connected to at least two bit lines each of which is connected to the sense node through at least one transistor, and the sense node is connected to the first node through at least one transistor.

60. (Currently Amended) The non-volatile semiconductor memory device according to claim 57,

wherein each of the bit line control circuits further includes a charging circuit and a voltage ~~setting~~ supplying circuit; and the first bit line is charged by the charging circuit before the predetermined period, the first voltage is applied to the sense node corresponding to the bit line control circuit storing data of the second logic level by the voltage ~~setting~~ supplying circuit, and the first voltage is not applied to the sense node corresponding to the bit line control circuit storing data of the first logic level by the voltage ~~setting~~ supplying circuit.

61. (Currently Amended) The non-volatile semiconductor memory device according to claim 60, wherein the bit line is not biased by any of the charging circuit and the voltage ~~setting~~ supplying circuit in a write operation.

62. (Previously Presented) The non-volatile semiconductor memory device according to claim 60, wherein the second bit line is not biased by the charging circuit when the first bit line is biased by the charging circuit.

63. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein the first voltage is a power supply voltage.

64. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein the first voltage is 0 V.

65. (Currently Amended) The non-volatile semiconductor memory device according to claim 28,

wherein: each of the bit line control circuits includes a data latch circuit and a voltage ~~setting~~ supplying circuit; the voltage ~~setting~~ supplying circuit includes a first transistor and a second transistor; the first transistor and the second transistor are connected in series; the data latch circuit stores data of the first logic level or the second logic level; a voltage level of a first node in the data latch circuit depends on the data stored in the bit line control circuit; and a voltage level of a gate of the second transistor reflects the voltage level of the first node in a voltage ~~setting~~ supplying operation; and the voltage ~~setting~~ supplying circuit sets a voltage level of the sense node corresponding to the bit line control circuit storing data of the second logic level.

66. (Currently Amended) The non-volatile semiconductor memory device according to claim 65, wherein a voltage level of a voltage supplied by the voltage ~~setting~~ supplying circuit is limited by voltage levels of gates of the first and the second transistors in the ~~first~~ voltage ~~setting~~ supplying operation.

67. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein a first bit line control circuit stores data of the first logic level in the predetermined period before the detection operation, and data of a logic level stored in the first bit line control circuit after the detection operation is dependent on a written state of the first memory cell corresponding to the first bit line control circuit.

68. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein a first data is stored in a first bit line control circuit in the predetermined period before the detection operation, and data of a logic level stored in the first bit line control circuit after the detection operation is dependent on the first data and a written state of a memory cell corresponding to the first bit line control circuit.

69. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein a second data of the second logic level is stored in a first bit line control circuit in the predetermined period before the detection operation, and data of a logic level stored in the second bit line control circuit after the detection operation is independent of a written state of a memory cell corresponding to the second bit line control circuit.

70. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein a write operation is performed after the detection operation, and a voltage level of a third bit line depends on data of a logic level stored in the bit line control circuit corresponding to the third bit line.

71. (Currently Amended) The non-volatile semiconductor memory device according to claim 28,

wherein: each of the plurality of bit line control circuits includes or is connected to a sense node; a voltage level of the sense node is sensed by the bit line control circuit to determine a detection result in a detection operation; and the sense node corresponding to the bit line control circuit storing data of the second logic level is set to the first voltage when the first voltage is supplied to the second bit line ~~is set to the first voltage~~ in the predetermined period.

72. (Currently Amended) The non-volatile semiconductor memory device according to claim 28,

wherein: each of the plurality of bit line control circuits includes or is connected to a sense node; a voltage level of the sense node is sensed by the bit line control circuit to determine a detection result in a detection operation; and when the first voltage is supplied to the second bit line ~~is set to the first voltage~~ in the predetermined period, the sense node corresponding to the bit line control circuit storing data of the first logic level is set to a voltage which is not lower than a second voltage of the first bit line.

73. (Previously Presented) The non-volatile semiconductor memory device according to claim 72, wherein the second voltage is not lower than the first voltage.

74. (Previously Presented) The non-volatile semiconductor memory device according to claim 28,

wherein: each of the plurality of bit line control circuits includes or is connected to a sense node; a voltage level of the sense node is sensed by the bit line control circuit to determine a detection result in a detection operation; and the sense node is the bit line.

75. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein one or more bit lines are connected to each of the plurality of bit line control circuits, at least one of the one or more bit lines is a selected bit line in one operation, the selected bit line corresponds to the first bit line or the second bit line, and at least two of all the selected bit lines in one cell array are adjacent to each other.

76. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein one or more bit lines are connected to each of the plurality of bit line control circuits, only one of the one or more bit lines is a selected bit line in one operation, the selected bit line corresponds to the first bit line or the second bit line, and at least two of all the selected bit lines in one cell array are adjacent to each other.

77. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein one or more bit lines are connected to each of the plurality of bit line control circuits, at least one of the one or more bit lines is a selected bit line in one operation, the selected bit line corresponds to the first bit line or the second bit line, and memory cells each of which is connected to each of at least two of all the selected bit lines in one cell array are adjacent to each other.

78. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein one or more bit lines are connected to each of the plurality of bit line control circuits, only one of the one or more bit lines is a selected bit line in one operation, the selected bit line corresponds to the first bit line or the second bit line, and memory cells each of which is connected to each of at least two of all the selected bit lines in one cell array are adjacent to each other.

79. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein third bit lines including two or more bit lines are selected simultaneously, each of the third bit lines is connected to at least one memory cell included in second memory cells, and written states of all of the second memory cells are detected simultaneously in the detection operation.

80. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein each of all bit lines in the non-volatile semiconductor memory device is connected to at least one memory cell included in second memory cells, and written states of all the second memory cells are detected simultaneously in the detection operation.

81. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein each of all bit lines in one memory cell array is connected to at least one memory cell included in second memory cells, and written states of all the second memory cells are detected simultaneously in the detection operation.

82. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein only one bit line is connected to each of the plurality of bit line control circuits, and all the bit lines in one cell array are simultaneously selected, and each of the bit lines corresponds to the first bit line or the second bit line.

83. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein only one bit line is connected to each of the plurality of bit line control circuits, and all the bit lines connected to all the bit line control circuits in one cell array are simultaneously selected, and each of the bit lines corresponds to the first bit line or the second bit line.

84. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein one or more bit lines are connected to each of the plurality of bit line control circuits, at least one of the one or more bit lines is a selected bit line in one operation, the selected bit line corresponds to the first bit line or the second bit line, and all the selected bit lines in one cell array are not adjacent to one another.

85. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein one or more bit lines are connected to each of the plurality of bit line control circuits, only one of the one or more bit lines is a selected bit line in one operation, the selected bit line corresponds to the first bit line or the second bit line, and all the selected bit lines in one cell array are not adjacent to one another.

86. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein first bit line control circuits including two or more bit line control circuits are selected simultaneously, and the first bit line control circuits perform the detection operation simultaneously.

87. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein first bit line control circuits including two or more bit line control circuits

storing data of the first logic level are included in selected bit line control circuits, and the first bit line control circuits perform the detection operation simultaneously.

88. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein first bit line control circuits including two or more bit line control circuits are selected simultaneously, and the first bit line control circuits perform an operation of charging selected bit lines corresponding to the first control circuits simultaneously.

89. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein the memory cell is a flash memory cell.

90. (Previously Presented) The non-volatile semiconductor memory device according to claim 28, wherein the memory cell is a NAND cell type EEPROM.

91. (Currently Amended) A non-volatile semiconductor memory device comprising:

a memory cell array including a plurality of memory cells **[[being]]** arranged in a matrix;

a word line connected to two or more memory cells arranged in a row direction;

a source line connected to two or more memory cells;

a row decoder circuit configured to supply a write verify voltage to the word line;

a plurality of bit lines each connected to two or more memory cells arranged in a column direction; and

a plurality of bit line control circuits each being provided for at least one of the bit lines, and each storing data of a first logic level or a second logic level,

wherein:

one or more of the bit lines are connected to each of the plurality of bit line control circuits, at least one of the one or more bit lines being selected in one operation;

a first bit line selected from the bit lines is connected to the bit line control circuit storing the first logic level, a second bit line selected from the bit lines is connected to the bit line control circuit storing the second logic level;

the bit line control circuit storing data of the first logic level performs a detection operation for detecting a written state of a first memory cell connected to the first bit line after a predetermined period [[after]] from completion of a charging operation for charging the first bit line; and

during the predetermined period, a first voltage is supplied to the second bit line ~~is set to a first voltage during the predetermined period~~.

92. (Previously Presented) The non-volatile semiconductor memory device according to claim 91, wherein only one of the one or more bit lines is selected in one operation.

93. (Previously Presented) The non-volatile semiconductor memory device according to claim 91, wherein the first voltage is a power supply voltage.

94. (Previously Presented) The non-volatile semiconductor memory device according to claim 91, wherein the first voltage is 0 V.

95. (Previously Presented) The non-volatile semiconductor memory device according to claim 91, wherein the memory cell is a flash memory cell.

96. (Previously Presented) The non-volatile semiconductor memory device according to claim 91, wherein the memory cell is a NAND cell type EEPROM.

97. (Currently Amended) A non-volatile semiconductor memory device comprising:

a memory cell array including a plurality of memory cells [[being]] arranged in a matrix;

a word line connected to two or more memory cells arranged in a row direction;

a source line connected to two or more memory cells;

a row decoder circuit configured to supply a write verify voltage to the word line;

a plurality of bit lines each connected to two or more memory cells arranged in a column direction; and

a plurality of bit line control circuits each being provided for at least one of the bit lines, each storing data of a first logic level or a second logic level, and each includes or is connected to a sense node,

wherein:

a voltage level of each of the sense nodes is sensed by the corresponding bit line control circuit to determine a detection result in a detection operation;

the bit line control circuit storing data of the first logic level performs the detection operation for detecting a written state of a first memory cell corresponding to the bit line control circuit storing data of the first logic level after a predetermined period [[after]] from completion of charging a first bit line corresponding to the bit line control circuit storing data of the first logic level; and

during the predetermined period, [[the]] a first voltage is supplied to ~~level of~~ each of the sense nodes corresponding to the bit line control circuit storing data of the second logic level ~~is set a first voltage~~.

98. (Previously Presented) The non-volatile semiconductor memory device according to claim 97, wherein each of the sense nodes is connected to the bit line through at least one transistor.

99. (Previously Presented) The non-volatile semiconductor memory device according to claim 97, wherein each of the sense nodes is the bit line.

100. (Previously Presented) The non-volatile semiconductor memory device according to claim 97, wherein the first voltage is a power supply voltage.

101. (Previously Presented) The non-volatile semiconductor memory device according to claim 97, wherein the first voltage is 0 V.

102. (Previously Presented) The non-volatile semiconductor memory device according to claim 97, wherein the memory cell is a flash memory cell.

103. (Previously Presented) The non-volatile semiconductor memory device according to claim 97, wherein the memory cell is a NAND cell type EEPROM.

104. (Currently Amended) A non-volatile semiconductor memory device comprising:

a memory cell array including a plurality of memory cells **[[being]]** arranged in a matrix;

a word line connected to two or more memory cells arranged in a row direction;

a source line connected to two or more memory cells;

a row decoder circuit configured to supply a write verify voltage to the word line;

a plurality of bit lines each connected to two or more memory cells arranged in a column direction; and

a plurality of bit line control circuits each being provided for at least one of the bit lines, each storing data of a first logic level or a second logic level, and each includes or is connected to a sense node,

wherein:

one or more bit lines are connected to each of the plurality of bit line control circuits, at least one of the one or more bit lines being selected in one operation;

a first bit line selected from the bit lines is connected to the bit line control circuit storing the first logic level;

a voltage level of each of the sense nodes is sensed by the corresponding bit line control circuit to determine a detection result in a detection operation;

the bit line control circuit storing data of the first logic level performs the detection operation for detecting a written state of a first memory cell connected to the first bit line <u>after</u> a predetermined period **[[after]]** <u>from</u> completion of charging the first bit line, and

during the predetermined period, **[[the]]** <u>a first</u> voltage ~~level of~~ <u>is supplied to</u> the sense node corresponding to each of the bit line control circuits storing data of the second logic level ~~is set to a first voltage~~.

105. (Previously Presented) The non-volatile semiconductor memory device according to claim 104, wherein only one of the one or more bit lines is selected in one operation.

106. (Previously Presented) The non-volatile semiconductor memory device according to claim 104, wherein each of the sense nodes is connected to the corresponding bit line through at least one transistor.

107. (Previously Presented) The non-volatile semiconductor memory device according to claim 104, wherein each of the sense nodes is the bit line.

108. (Previously Presented) The non-volatile semiconductor memory device according to claim 104, wherein the first voltage is a power supply voltage.

109. (Previously Presented) The non-volatile semiconductor memory device according to claim 104, wherein the first voltage is 0 V.

110. (Previously Presented) The non-volatile semiconductor memory device according to claim 104, wherein the memory cell is a flash memory cell.

111. (Previously Presented) The non-volatile semiconductor memory device according to claim 104, wherein the memory cell is a NAND cell type EEPROM.

112. (Currently Amended) A non-volatile semiconductor memory device comprising:

a memory cell array including a plurality of memory cells **[[being]]** arranged in a matrix;

a word line connected to two or more memory cells arranged in a row direction;

a source line connected to two or more memory cells;

a row decoder circuit configured to supply a write verify voltage to the word line;

a plurality of bit lines each connected to two or more memory cells arranged in a column direction; and

a plurality of bit line control circuits each being provided for at least one of the bit lines, and each storing data of a first logic level or a second logic level,

wherein the bit line control circuit storing data of the first logic level performs a detection operation for detecting a written state of a first memory cell corresponding to the bit

line control circuit storing data of the first logic level after a predetermined period [[after]] from completion of a charging operation for charging a first bit line corresponding to the bit line control circuit storing data of the first logic level, and

during the predetermined period, a second bit line corresponding to the bit line control circuit storing data of the second logic level does not have a voltage level reflecting a written state of a second memory cell corresponding to the bit line control circuit storing data of the second logic level.

113. (Previously Presented) The non-volatile semiconductor memory device according to claim 112, wherein the memory cell is a flash memory cell.

114. (Previously Presented) The non-volatile semiconductor memory device according to claim 112, wherein the memory cell is a NAND cell type EEPROM.

115. (Currently Amended) A non-volatile semiconductor memory device comprising:

a memory cell array including a plurality of memory cells [[being]] arranged in a matrix;

a word line connected to two or more memory cells arranged in a row direction;

a source line connected to two or more memory cells;

a row decoder circuit configured to supply a write verify voltage to the word line;

a plurality of bit lines each connected to two or more memory cells arranged in a column direction; and

a plurality of bit line control circuits each being provided for at least one of the bit lines, and each storing data of a first logic level or a second logic level,

wherein one or more bit lines are connected to each of the plurality of bit line control circuits, at least one of the one or more bit lines is selected in one operation,

a first bit line selected from the bit lines is connected to the bit line control circuit storing the first logic level, a second bit line selected from the bit lines is connected to the bit line control circuit storing the second logic level,

the bit line control circuit storing data of the first logic level performs a detection operation for detecting a written state of a first memory cell connected to the first bit line after

a predetermined period [[after]] from completion of a charging operation for charging the first bit line, and

during the predetermined period, the second bit line does not have a voltage level reflecting a written state of a second memory cell connected to the second bit line.

116. (Previously Presented) The non-volatile semiconductor memory device according to claim 115, wherein only one of the one or more bit lines is selected in one operation.

117. (Previously Presented) The non-volatile semiconductor memory device according to claim 115, wherein the memory cell is a flash memory cell.

118. (Previously Presented) The non-volatile semiconductor memory device according to claim 115, wherein the memory cell is a NAND cell type EEPROM.

119. (Currently Amended) A non-volatile semiconductor memory device comprising:

a memory cell array including a plurality of memory cells [[being]] arranged in a matrix;

a word line connected to two or more memory cells arranged in a row direction;

a source line connected to two or more memory cells;

a row decoder circuit configured to supply a write verify voltage to the word line;

a plurality of bit lines each connected to two or more memory cells arranged in a column direction; and

a plurality of bit line control circuits each being provided for at least one of the bit lines, each storing data of a first logic level or a second logic level, and each includes or is connected to a sense node,

wherein:

a voltage level of each of the sense nodes is sensed by the corresponding bit line control circuit to determine a detection result in a detection operation;

the bit line control circuit storing data of the first logic level performs the detection operation for detecting a written state of a first memory cell corresponding to the bit line control circuit storing data of the first logic level after a predetermined period [[after]] from

completion of charging a first bit line corresponding to the bit line control circuit storing data of the first logic level; and

during the predetermined period, each of the sense nodes corresponding to the bit line control circuit storing data of the second logic level does not have a voltage level reflecting a written state of a second memory cell corresponding to the bit line control circuit storing data of the second logic level.

120. (Previously Presented) The non-volatile semiconductor memory device according to claim 119, wherein each of the sense nodes is connected to the corresponding bit line through at least one transistor.

121. (Previously Presented) The non-volatile semiconductor memory device according to claim 119, wherein each of the sense nodes is the bit line.

122. (Previously Presented) The non-volatile semiconductor memory device according to claim 119, wherein the memory cell is a flash memory cell.

123. (Previously Presented) The non-volatile semiconductor memory device according to claim 119, wherein the memory cell is a NAND cell type EEPROM.

124. (Currently Amended) A non-volatile semiconductor memory device comprising:

a memory cell array including a plurality of memory cells **[[being]]** arranged in a matrix;

a word line connected to two or more memory cells arranged in a row direction;

a source line connected to two or more memory cells;

a row decoder circuit configured to supply a write verify voltage to the word line;

a plurality of bit lines each connected to two or more memory cells arranged in a column direction; and

a plurality of bit line control circuits each being provided for at least one of the bit lines, each storing data of a first logic level or a second logic level, and each includes or is connected to a sense node,

wherein:

one or more bit lines are connected to each of the plurality of bit line control circuits, at least one of the one or more bit lines being selected in one operation;

a first bit line selected from the bit lines is connected to the bit line control circuit storing the first logic level, a second bit line selected from the bit lines is connected to the bit line control circuit storing the second logic level;

a voltage level of each of the sense nodes is sensed by the corresponding bit line control circuit to determine a detection result in a detection operation;

the bit line control circuit storing data of the first logic level performs the detection operation for detecting a written state of a first memory cell connected to the first bit line after a predetermined period [[after]] from completion of charging the first bit line; and

during the predetermined period, each of the sense nodes corresponding to the bit line control circuit storing data of the second logic level does not have a voltage level reflecting a written state of a second memory cell connected to the second bit line.

125. (Previously Presented) The non-volatile semiconductor memory device according to claim 124, wherein only one of the one or more bit lines is selected in one operation.

126. (Previously Presented) The non-volatile semiconductor memory device according to claim 124, wherein each of the sense nodes is connected to the bit line through at least one transistor.

127. (Previously Presented) The non-volatile semiconductor memory device according to claim 124, wherein each of the sense nodes is the bit line.

128. (Previously Presented) The non-volatile semiconductor memory device according to claim 124, wherein the memory cell is a flash memory cell.

129. (Previously Presented) The non-volatile semiconductor memory device according to claim 124, wherein the memory cell is a NAND cell type EEPROM.